	**SULTAN QABOOS UNIVERSITY** **COLLEGE OF SCIENCE** **DEPARTMENT OF COMPUTER SCIENCE** **BACHELOR OF SCIENCE IN COMPUTER SCIENCE** **COURSE OUTLINE**

I. COURSE INFORMATION			
COURSE CODE	COMP3501		
COURSE TITLE	Computer Organization & Assembly Language		
OMAN QUALIFICATION FRAMEWORK (OQF) LEVEL	7		
CREDIT HOURS	3		
CONTACT HOURS	4		
PRE-REQUISITES	COMP2101, ECCE3206, LANC2058		
CO-REQUISITES	-		
EQUIVALENT COURSES	COMP3518		
INCOMPATIBLE COURSES			
COURSE CATEGORY	☐ University Requirement	☐ University Elective	
	☐College Requirement	☐ College Elective	
	☐ Department Requirement	☐ Department Elective	
	☒ Major Requirement	☐ Major Elective	
	☐ Specialization Requirement	☐ Specialization Elective	
	☐ Other (specify):		
COURSE OWNER	College: Science	Department: Computer Science	
	Center:	Unit:	
DELIVERY MODE	☒ Face to Face	☐ Blended	☐ Online
COURSE TYPE	☐ Lecture	☒ Lecture/Lab	

	☐ Lecture/Seminar	☐ Lecture/Studio	
	☐ Lecture/Tutorial	☐ Lecture/Lab/Tutorial or Seminar	
	☐Tutorial	☐ Laboratory (Practical)	
	☐ Field or Work Placement	☐ Studio	
	☐Seminar	☐ Internship	
	☐ Workshop	☐ Project	
	☐ Thesis	☐ Other (specify):	
LANGUAGE OF INSTRUCTION	English		
COURSE DESCRIPTION	The objective of the course is to introduce the students to the fundamentals of computer organization and assembly language programming. The course topics include data representations, instruction set architectures, assembly language programming, memory hierarchy, cache memory, virtual memory, input/output and storage systems, and introduction to parallel architectures. Students will practice assembly language programming of a selected architecture.		
TEACHING AND LEARNING STRATEGIES	☐ Augmented Reality	☐ Flipped Classroom	
	☒ Blended Learning	☒ Problem-Based Learning	
	☐ Discovery-Based Learning	☐ Project-Based Learning	
	☐ Student-Led Learning	☐ Team-Based Learning	
	☐ Work-Based Learning	☐ Other (specify):	
ASSESSMENT COMPONENT AND WEIGHT	☒ In-term examination(s) (20 %)	☐ Quizzes (%)	☐Other (specify): lab exercises (%)
	☒ Homework assignments (20 %)	☐ Project (%)	
	☒ Final examination (40 %)	☒ Practical/ Lab (20%)	
TEXTBOOKS AND EDUCATIONAL MATERIAL	1. Linda Null and Julia Lobur, ***The Essentials of Computer Organization and Architecture***, Third Edition, John and Barlett Publishers (ISBN-13: 9781449600068), 2012. 2. Kip Irvine, ***Assembly Language for x86 Processors***, 6th Edition, Prentice Hall, 2011.		
GRADING METHOD	☒ A-F Scale	☐ Pass/Not Pass	☐ Other (specify):

GRADING METHOD DESCRIPTION			
A-F GRADING SCALE:	**Range**	**Letter Grade**	**Description**
	90 – 100	A	**Exceptional performance:** All course objectives achieved and met in a consistently outstanding manner.
	86 – 89.9	A-	
	81– 85.9	B+	**Very Good Performance:** The majority of the course objectives achieved (majority being at least two-thirds) and met in a consistently thorough manner.
	77 – 80.9	B	
	73 – 76.9	B-	
	68 – 72.9	C+	**Satisfactory Performance:** At least most of course objectives have been achieved and met satisfactorily.
	64 – 67.9	C	
	60 – 63.9	C-	
	55 – 59.9	D+	**Minimally Acceptable Performance:** The course objectives met at a minimally acceptable level.
	50 – 54.9	D	
	0 – 49.9	F	**Unacceptable performance:** The course objectives not met at a minimally acceptable level.
PASS/NOT PASS:			
OTHER:			

II. SEMESTER INFORMATION			
SEMESTER/YEAR	Spring 2025	**SECTION(S)**	01 and 02
DAY AND TIME	**Section 01** • Lecture:Sun 14:15-16:05, CMT/D12 • Lab: Tue 14:15-16:05, SCI/0019B **Section 02** • Lecture:Mon 14:15-16:05, CMT/D16 • Lab: Wed 14:15-16:05, SCI/0022	**VENUE(S)**	**Section 01** • Lec.:Sun CMT/D12 • Lab.:Tue, SCI/0019B **Section 02** • Lec.:Mon CMT/D16 • Lab.:Wed SCI/0022
COURSE COORDINATOR	Dr. Amjad Mohamed Al-Tobi	**COURSE TEAM**	
COORDINATOR OFFICE	Office No. 1049, CIS.	**OFFICE HOURS**	Sun, Tue: 11-12
COORDINATOR EXTENSION	2821	**COORDINATOR EMAIL**	amjad@squ.edu.om

III. Alignment of Course Learning Outcomes (CLO), Program Learning Outcomes (PLO), Graduate Attributes (GA), and Oman Qualification Framework (OQF) Characteristics			
CLO	**PLO / SO**	**SQU Graduate Attributes**	**OQF Characteristics**
1. Describe the basic functional components of a computer system, their operation and interconnection.	**SO1**	**A**	**1,3**
2. Define several approaches to processor design: non-pipelined, pipelined, superscalar, RISC, CISC, multiprocessor.	**SO1**	**A**	**1,3**
3. Use data representation, instruction set, addressing modes and register organization.	**SO1**	**A**	**1,3**
4. Explain memory organization, cache memory, and storage systems.	**SO1**	**A**	**1,3**
5. Describe I/O system and interconnection structures of computers, I/O driven interrupts, and interrupt handling.	**SO1**	**A**	**1,3**
6. Describe parallel processing architectures.	**SO1**	**A**	**1,3**
7. Use the process of assembling, linking, executing, and debugging assembly programs.	**SO1,SO2**	**A,B**	**1,2,3**
8. Develop assembly language programs that include implementations of arithmetic expressions, flow control constructs (sequential, conditional and iterative) and subroutines.	**SO1,SO2**	**A,B**	**1,2,3**
9. Identify the tradeoff factors affecting the design and performance of a computer system component (e.g., ISA, pipelining speedups, memory hierarchy, cache memory and I/O control methods).	**SO2**	**A**	**1**

IV. Course Learning Outcomes (CLOs) and Assessment Criteria and Methods (for each CLO)		
CLO1: Describe the basic functional components of a computer system, their operation and interconnection.		
Assessment Criteria (to achieve this objective, the student must)		**Assessment Methods**
A)	Demonstrates a thorough understanding of the functional components (e.g., CPU, memory, I/O systems) and their respective operations.	Homework, Midterm, Final
B)	Provides a clear and accurate description of how these components interconnect and communicate with each other in a computer system.	
C)	Applies knowledge to explain how component interconnections influence overall system performance.	

CLO2: Define several approaches to processor design: non-pipelined, pipelined, superscalar, RISC, CISC, multiprocessor.		
ASSESSMENT CRITERIA (TO ACHIEVE THIS OBJECTIVE, THE STUDENT MUST)		**ASSESSMENT METHODS**
A)	Identifies and clearly defines the characteristics of non-pipelined, pipelined, superscalar, RISC, CISC, and multiprocessor designs.	Homework, Final
B)	Compares and contrasts these processor design approaches, highlighting strengths and weaknesses.	
CLO3: Use data representation, instruction set, addressing modes and register organization.		
ASSESSMENT CRITERIA (TO ACHIEVE THIS OBJECTIVE, THE STUDENT MUST)		**ASSESSMENT METHODS**
A)	Demonstrates accurate and comprehensive knowledge of data representation, including binary, hexadecimal, and other forms.	Homework, Midterm, Final
B)	Identifies and utilizes instruction sets, addressing modes, and register organization when designing and interpreting assembly code.	
C)	Applies data representation and instruction set principles in assembly language programming exercises.	
CLO4: Explain memory organization, cache memory, and storage systems.		
ASSESSMENT CRITERIA (TO ACHIEVE THIS OBJECTIVE, THE STUDENT MUST)		**ASSESSMENT METHODS**
A)	Provides a detailed explanation of different types of memory organization, including cache memory and hierarchical storage systems.	Homework, Midterm, Final
B)	Demonstrates an understanding of how cache memory and storage systems improve computer performance.	
C)	Analyzes the implications of various memory organization techniques on system speed and efficiency.	
CLO5: Describe I/O system and interconnection structures of computers, I/O driven interrupts, and interrupt handling.		
ASSESSMENT CRITERIA (TO ACHIEVE THIS OBJECTIVE, THE STUDENT MUST)		**ASSESSMENT METHODS**
A)	Describes the role and functioning of I/O systems and interconnection structures within a computer.	Homework, Midterm, Final
B)	Demonstrates a clear understanding of I/O-driven interrupts, including how they are triggered and handled.	

CLO6: Describe parallel processing architectures.		
ASSESSMENT CRITERIA (TO ACHIEVE THIS OBJECTIVE, THE STUDENT MUST)		**ASSESSMENT METHODS**
A)	Identifies and clearly explains the different types of parallel processing architectures (e.g., SIMD, MIMD).	Homework, Final
B)	Evaluates the benefits and limitations of parallel processing architectures in comparison to traditional architectures.	
CLO7: Use the process of assembling, linking, executing, and debugging assembly programs.		
ASSESSMENT CRITERIA (TO ACHIEVE THIS OBJECTIVE, THE STUDENT MUST)		**ASSESSMENT METHODS**
A)	Demonstrates a complete understanding of the process of assembling, linking, executing, and debugging assembly language programs.	Homework, Lab Test
B)	Assembles, links, executes, and debugs assembly programs during laboratory exercises and assessments.	
CLO8: Develop assembly language programs that include implementations of arithmetic expressions, flow control constructs (sequential, conditional and iterative) and subroutines.		
ASSESSMENT CRITERIA (TO ACHIEVE THIS OBJECTIVE, THE STUDENT MUST)		**ASSESSMENT METHODS**
A)	Implements arithmetic expressions in assembly language.	Homework, Lab Test
B)	Uses flow control constructs, including sequential, conditional, and iterative operations, in assembly programs.	
C)	Develops and tests subroutines that are used in larger assembly programs, ensuring functional accuracy.	
CLO9: Identify the tradeoff factors affecting the design and performance of a computer system component (e.g., ISA, pipelining speedups, memory hierarchy, cache memory and I/O control methods).		
ASSESSMENT CRITERIA (TO ACHIEVE THIS OBJECTIVE, THE STUDENT MUST)		**ASSESSMENT METHODS**
A)	Identifies and clearly explains various trade-off factors in system design (e.g., performance vs. cost, speed vs. complexity).	Homework, Midterm, Final
B)	Evaluates how design decisions impact overall system performance, particularly in relation to pipelining, memory hierarchy, and cache memory.	
C)	Applies understanding of trade-offs to propose optimizations or design choices that improve system performance while balancing costs and other constraints.	

V. COURSE CONTENT AND SCHEDULE				
WEEK	**LECTURES #**	**TOPICS/ SUBJECTS**	**READINGS/ CHAPTERS**	**REMARKS (e.g., ASSESSMENTS)**
1	Lecture 1 Lab 1	L1: Introduction: main components of a computer, historical development, computer level hierarchy, von-Neumann model, non-von Neumann models. **Lab1: X86 architecture: general concepts, x86 architecture details, x86 memory management, components of a typical x86 computer, I/O system.**	Textbook 1: 1.1-1.2, 1.5-1.8 Textbook 2: 2.1 – 2.5	Midterm, Final
2	Lecture 2 Lab 2	L2: Data Representation in Computer Systems: positional numbering systems, converting between bases. **Lab2: Microsoft Macro Assembler (MASM): basic elements of MASM assembly language, example: adding and subtracting integers, assembling, linking, debugging, and running programs.**	Textbook 1: 2.1 – 2.3 Textbook 2: 3.1 – 3.3	HW1, Midterm, Lab Test, Final
3	Lecture 3 Lab 3	L3: Data Representation in Computer Systems: signed integer representation, floating-point representation, character codes. **Lab3: Microsoft Macro Assembler: defining data, symbolic constants.**	Textbook 1: 2.4 – 2.6 Textbook 2: 3.4 – 3.5	HW1, Midterm, Lab Test, Final
4	Lecture 4 Lab 4	L4: Introduction to a Simple Computer: CPU basics and organization, the bus, clocks, I/O subsystem, memory organization and addressing. **Lab4: Data Transfers, Addressing, and Arithmetic: data transfer instructions, addition and subtraction.**	Textbook 1: 4.1 – 4.6 Textbook 2: 4.1 – 4.2	HW2, Midterm, Lab Test, Final
5	Lecture 5	L5: Introduction to a Simple Computer: interrupts, simple	Textbook 1: 4.7 – 4.12	HW2, Midterm, Lab Test,

	Lab 5	computer architecture (MARIE), instruction processing, a simple program, a discussion on assemblers, extending the instruction set. **Lab5: Data Transfers, Addressing, and Arithmetic: data transfer instructions, addition and subtraction.**	Textbook 2: 4.1 – 4.2	Final
6	Lecture 6 Lab 6	L6: ISAs: instruction formats, instruction types, addressing. **Lab6: Data Transfers, Addressing, and Arithmetic: data-related operators and directives, indirect addressing, JMP and LOOP instructions.**	Textbook 1: 5.1 – 5.4 Textbook 2: 4.3 – 4.5	HW2, Midterm, Lab Test, Final
7	Lecture 7 Lab 7	L7: Instruction Set Architectures: instruction pipelining, examples. **Lab7: Stack Operations and Procedures: linking to an external library, the book's link library, stack operations.**	Textbook 1: 5.5 – 5.6 Textbook 2: 5.1 – 5.4	HW3, Midterm, Lab Test, Final
8	Lecture 8 Lab 8	L8: Memory: memory types, memory hierarchy. **Lab8: Stack Operations and Procedures: defining and using procedures, program design using procedures.**	Textbook 1: 6.1 – 6.3 Textbook 2: 5.5 – 5.6	HW3, Midterm, Lab Test, Final
9	Lecture 9 Lab 9	L9: Midterm Exam. **Lab9: Conditional Processing: Boolean and comparison instructions.**	Textbook 2: 6.1 – 6.2	HW3, Lab Test, Final
10	Lecture 10 Lab 10	L10: Memory: cache memory, real-world example. **Lab10: Conditional Processing: conditional jumps, conditional loop instructions, conditional structures.**	Textbook 1: 6.4, 6.6 Textbook 2: 6.3 – 6.5	HW4, Lab Test, Final
11	Lecture 11	L11: System Software: operating systems.	Textbook 1: 8.1 – 8.2	HW4, Lab Test, Final

	Lab 11	**Lab11: Integer Arithmetic: shift and rotate instructions and their applications.**	Textbook 2: 7.1-7.3	
12	Lecture 12 Lab 12	L12: System Software: protected environments, programming tools. **Lab12: Integer Arithmetic: multiplication and division instructions, extended addition and subtraction.**	Textbook 1: 8.3-8.4 Textbook 2: 7.4-7.5	HW4, Lab Test, Final
13	Lecture 13 Lab 13	L13: Alternative Architectures: RISC machines. **Lab13: Practice for Lab Test**	Textbook 1: 9.1 – 9.2	Lab Test, Final
14	Lecture 14 Lab 14	L14: Alternative Architectures: Flynn's taxonomy, parallel and multiprocessor architectures. **Lab14: Lab Test**	Textbook 1: 9.3 – 9.4	Final
15	Lecture 15 Lab 15	L15: Review. **Lab15: Review.**		Final

VI. Additional Information (e.g., Rubrics, etc.)

Assessment Plan:

Item	Date Out	Due Date	Weight
HW1	W3	W4	5%
HW2	W5	W7	5%
Midterm	W8 (Thu 27/03/2025, 13:00-13:00)		20%
HW3	W8	W9	5%
HW4	W10	W11	5%
Lab Test	W13 (Thu 01/05/2025, 13:00-13:00)		20%
Final Exam	Thu 29/05/2025, 11:30-14:30		40%

Department's Late Submission Policy:

(a) 1-24 hours: 25% of the mark will be deducted.

(b) > 24 hours: Not accepted.

Department's Policy for Dealing with Cheating:

It is essential that each student solves all programming assignments, lab tests and exams individually unless instructed otherwise, e.g., for group projects. Copying, plagiarism, collusion, switching, and falsification are violations of the university academic regulations. Students involved in such acts will be severely penalized. The department has adopted a firm policy on this issue. A zero mark will be assigned the first time a student is caught involved in copying and his/her name will be added to a watch list maintained by the Head of Department. Further repeated involvements in copying will cause the student to get an F grade in that course. This is in line with the university academic regulations.

VII. STUDENTS RESPONSIBILITIES	
It is the student's responsibility to know and comply with all University Academic Regulations relevant to participation in this course. These regulations specifically include attendance requirements and student academic code of conduct.	
ACADEMIC INTEGRITY	The University expects the students to approach their academic endeavors with the highest academic integrity. Please refer to the **Undergraduate Academic Regulations**.
ADD AND DROP	Students who wish to drop or add the course should review the **Undergraduate Academic Regulations**.
ATTENDANCE	Sultan Qaboos University has a clear requirement for students to attend courses, detailed in the **Undergraduate Academic Regulations**.
ASSESSMENT AND GRADING	To ensure the provision of a sound and fair assessment and grading, please review the **Undergraduate Academic Regulations**.
GRADE APPEAL	Students who wish to appeal their grades should review the **Undergraduate Academic Regulations**.
CLASSROOM POLICIES	Students are expected to dress professionally during class time as required by the University. Use of phones or any other electronic devices in the classroom during class time is strictly prohibited. Unauthorized use may lead to faculty member confiscation of the device for the remainder of the class. Behavior that persistently or grossly interferes with classroom activities is considered disruptive behavior and may be subject to disciplinary action. A student responsible for disruptive behavior may be required to leave the class.
LATE AND MAKE-UP WORK	Students are required to meet the course objectives by submitting coursework no later than the assigned due date. Students may be allowed to submit late work if approved by the course coordinator. Assignments submitted after the due date may be penalized.
MISSED EVALUATIONS	All quizzes, tests, clinical evaluations, and exams must be completed by the date they are assigned. If a quiz, test, or exam is missed due to a documented emergency situation (e.g., medical emergency, death in the immediate family), it is the student's responsibility to contact the instructor.
OTHER	

Course Outline Appendix

1. Program Learning Outcomes

SO1. Analyze a complex computing problem and to apply principles of computing and other relevant disciplines to identify solutions.

SO2. Design, implement, and evaluate a computing-based solution to meet a given set of computing requirements in the context of the program's discipline.

SO3. Communicate effectively in a variety of professional contexts.

SO4. Recognize professional responsibilities and make informed judgments in computing practice based on legal and ethical principles.

SO5. Function effectively as a member or leader of a team engaged in activities appropriate to the program's discipline.

SO6. Apply computer science theory and software development fundamentals to produce computing-based solutions.

2. SQU Graduate Attributes and Competencies for Undergraduate Studies

Graduate Attributes	Graduate competencies for Undergraduate Studies
A. Cognitive Capabilities: The graduate has sufficient general and specialized theoretical knowledge that enables him/her to deal well with his/her specialty and other related fields.	1. Demonstrates familiarity and works with advanced specialized knowledge in the area of specialization.
	2. Demonstrates a general understanding of the relationship of advanced specialized knowledge with knowledge in other relevant professional fields and aspects.
	3. Demonstrates a comprehensive understanding of the theories, principles, and methods used in his/her specialty, and how to create and apply new knowledge.
	4. Demonstrates general knowledge of the legal environment and necessary relevant regulatory

	frameworks.
	5. Shows awareness of contemporary literature and research.
B. Skill and Professional Capability: The graduate has sufficient skill and practical experience that enables him/her to perform all tasks related to the specialization and other related fields.	1. Applies concepts, theories, and investigative methods to synthesize and interpret information to evaluate conclusions.
	2. Applies appropriate research methods and techniques and employs digital knowledge
	3. Evaluates and critiques information independently
	4. Uses cognitive and technical skills to analyze complex issues and develop appropriate solutions.
	5. Initiates new ideas or processes in the professional, educational or research context.
C. Effective Communication: The graduate has the ability to communicate effectively with others to achieve the desired results	1. Explains, presents, and adapts information to suit the recipients.
	2. Employs appropriate information and communication technology to collect and analyze information.
D. Autonomy and Leadership: The graduate has the ability to lead, make decisions and take responsibility for decisions.	1. Performs advanced professional activities independently.
	2. Demonstrates leadership skills.
	3. Takes professional responsibility.
	4. Assumes full accountability for the tasks and their output.
E. Responsibility and Commitment: The graduate appreciates the importance of available resources and deals with them	1. Manages time and other resources assigned to accomplishing tasks effectively and responsibly.
	2. Demonstrates effective practices when working in teams.

effectively and is committed to the ethics of the profession and society.	3. Demonstrates advanced levels of understanding of values and ethics relevant to the specialization, profession and local and international society and promotes them among others.
	4. Works within the professional, institutional, and specialization guiding frameworks and strategic plans.
	5. Interacts with community affairs positively and preserves national identity.
F. Development and Innovation: The graduate has a passion for development and innovation in the field of specialization.	1. Demonstrates the ability to independently manage learning tasks, with an awareness of how to develop and apply new knowledge.
	2. Utilizes specialized knowledge and skills for entrepreneurship.
	3. Utilizes creative and innovative skills in the field of specialization.

3. OQF CHARACTERISTICS

1. Knowledge
2. Skills
3. Communication, Numeracy, and Information and Communication Technology Skills.
4. Autonomy and Responsibility
5. Employability and Values
6. Learning to learn